(54) Apparatus and methods for transmitting data

(57) DVD reproducing apparatus (100) transmits variable-bit rate data, on a digital serial bus (300) at a predetermined transmission rate, by reproducing data from a record medium (1) in accordance with a control signal to produce the variable rate data. The data rate of the variable rate data is detected (8) at predetermined intervals of time, the rate of transmission of the variable rate data is established in accordance with the detected data rate, and the variable rate data is transmitted in accordance with the established transmission rate. The DVD reproducing apparatus (100) may include an MPEG decoder (6) which MPEG decodes the reproduced data and which generates the control signal in accordance with amounts of data stored within various buffers, such control signal being utilized to control the reproduction of the data from the record medium (1). A receiver, e.g., a digital television (200), having an MPEG decoder (9) therein receives the transmitted data and MPEG decodes the data, but such MPEG decoder (9) does not generate a control signal similar to the previously generated control signal in order to prevent underflow/overflow of the memories therein. In another embodiment, the DVD reproducing apparatus (100) does not include an MPEG decoder, but the receiving device's MPEG decoder (9) generates a control signal that is transmitted back to the DVD reproducing apparatus (100) in order to prevent underflow/overflow of the memories within the receiving device's MPEG decoder.
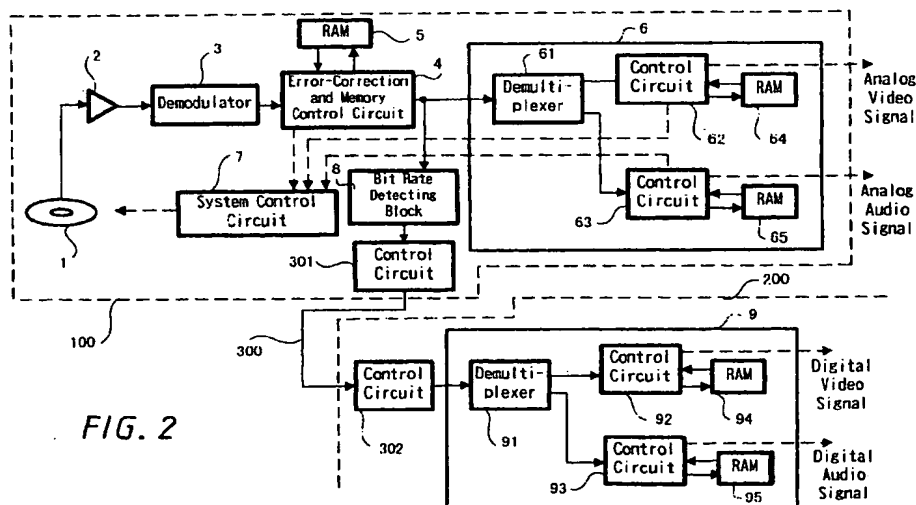
FIG. 2

EP 0 825 783 A2

Description

The present invention relates to apparatus and methods for transmitting data and, more particularly, to apparatus and methods for transmitting variable-bit rate data on a transmission line at a predetermined transmission rate.

As is known, various types of digital video-audio equipment, for example, DVD reproducing devices, digital VTRs, digital televisions, etc., are currently available for consumer use. Several such devices reproduce or receive digital video/audio signals, convert those signals into analog signals, and supply the analog signals to analog-type video/audio equipment. It is also generally desirable to supply from such equipment digital video/audio signals to, for example, a personal computer, a digital television receiver, or other type of digital device.

The communication system IEEE-1394 is a digital serial bus which has been proposed as a means for transmitting such digital video/audio signals between digital devices. Referring to Fig. 1 of the drawings, an exemplary block diagram of an IEEE-1394 system that includes an IEEE-1394 bus 901 and various digital devices 902-907 is shown. In the exemplary block diagram, the IEEE-1394 bus is coupled between a DVD reproducing apparatus 902, a digital VCR 903, a digital broadcasting receiver 904, a digital television receiver 905, a digital television receiver 906 and a personal computer 907. As shown, digital video/audio data is supplied from DVD reproducing apparatus 902 via the IEEE-1394 bus to digital television receiver 906, and digital video/audio data supplied from digital broadcasting 904 is supplied via bus 901 to digital television receiver 905. Given an IEEE-1394 bus with a transmission rate of, for example, 100 Mbps, and video/audio data is organized into "units" of data, then in accordance with IEEE-1394 standard, 4915 units of data can be transmitted during each 125 μsec transmission cycle of the bus. In accordance with this standard, the number of units transmitted corresponds to the bit rate of the signal to be transmitted. For example, to realize a communication speed of approximately 10 Mbps, which corresponds to the mean bit rate of a typical video signal, then approximately 1200 units are needed. However, to realize a communication speed of approximately 2 Mbps, which is the mean bit rate of an audio signal, then approximately 704 units are needed.

One limitation of the above discussed IEEE-1394 standard is that signals are transmitted only after their transmission rate (i.e., bit rate) is determined. However, DVD reproducing devices that employ MPEG encoders/decoders reproduce digital video/audio data at a variable rate and, thus, an IEEE 1394-bus previously has been unable to transmit variable rate data reproduced from such devices.

Respective aspects of the present invention are set out in claims 1, 5, 10, 13, 17, 22, 25, 29 and 34.

A preferred embodiment provides apparatus and methods for transmitting digital video/audio data which overcome the shortcomings of the above described system.

The preferred apparatus and methods are operable to transmit variable rate digital video/audio data in accordance with the IEEE-1394 standard.

In accordance with one embodiment of the present invention, apparatus and method are provided for detecting a data rate of variable rate data at predetermined intervals of time, establishing a rate of transmission of the variable rate data in accordance with the detected data rate, and transmitting in accordance with the established transmission rate the variable rate data on a transmission line that requires the transmission rate to be predetermined.

As one aspect of the present invention, a bandwidth of the transmission line that is required to transmit the variable rate data having the detected data rate is secured.

As a feature of this aspect, given a transmission line with a plurality of transmission cycles, the data rate of the variable rate data to be transmitted during each of the cycles is detected.

As another feature of this aspect, a new bandwidth is secured for each cycle of the transmission line in accordance with the detected data rate of the variable rate data to be transmitted during the respective cycle.

In accordance with another embodiment of the present invention, apparatus and method are provided for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal, processing the produced variable rate signal (e.g., by an MPEG decoder), generating the control signal in accordance with a condition of processing of the produced variable rate signal, and transmitting the variable rate signal on the transmission line.

As one aspect of this embodiment, the transmitted variable rate signal is received and processed in a similar manner as that of the produced variable rate signal (e.g., by a second MPEG decoder), but such second processing does not generate a control signal (similar to the earlier generated control signal) that represents a condition of the second processing.

In accordance with a further embodiment of the present invention, apparatus and method are provided for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal, transmitting from a transmission side the variable rate signal on the transmission line, receiving the variable rate signal transmitted on the transmission line, processing the received transmitted variable rate signal, generating the control signal in accordance with a condition of processing of the received transmitted variable rate signal, transmitting the generated control signal on the transmission line, and receiving at the transmission side the transmitted control signal, wherein the received transmitted control signal is

utilized to control the reproducing of a signal from the record medium.

Exemplary embodiments of the invention are described hereinafter, by way of example only, with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a system employing an IEEE-1394 digital serial bus;

Fig. 2 is a block diagram of a data transmission apparatus in accordance with an embodiment of the present invention;

Fig. 3 is a block diagram of a data transmission apparatus in accordance with another embodiment of the present invention;

Fig. 4 is a simplified block diagram of the device shown in Fig. 2;

Fig. 5 is a simplified block diagram of the device shown in Fig. 3;

Fig. 6 is a flow chart of the operation of a bit rate detecting block;

Fig. 7 is a block diagram of control circuits;

Fig. 8 schematically illustrates the data structure of an Iso packet; and

Fig. 9 is a schematic illustration of the transmission bandwidth of a digital serial bus that is transmitting data in accordance with embodiments of the present invention.

Figs. 2 and 3 illustrate different embodiments of the data transmission apparatus of the present invention, wherein Fig. 2 illustrates a DVD reproducing apparatus 100 that includes an MPEG decoder 6, and Fig. 3 illustrates a DVD reproducing apparatus 100 that does not include an MPEG decoder. As will be discussed, DVD reproducing apparatus 100 shown in both Figs. 2 and 3 are coupled via an IEEE-1394 digital serial bus 300 to an MPEG decoder 9, included in, for example, a digital television receiver.

Referring first to the embodiment of the present invention shown in Fig. 2, DVD reproducing apparatus 100 is operable to reproduce digital video/audio data from a digital video disk, decode the reproduced data in MPEG decoder 6, and supply the decoded data as respective analog video and audio signals. The analog video and audio signals may be supplied to, for example, an analog television receiver, an analog recording device, etc. DVD reproducing apparatus 100 further is operable to transmit the reproduced digital video/audio data via bus 300 to an external MPEG decoder 9 which decodes the transmitted signal and supplies digital video and audio signals as an output.

DVD reproducing apparatus 100 embodying the present invention reproduces digital video/audio data from a digital video disk in a reproducing device 1 which supplies the reproduced data via an amplifier circuit 2 to a demodulator 3 which demodulates the reproduced signal. The demodulated signal is supplied to an error correction and memory control circuit 4 which stores the supplied signal in a random access memory 5 and corrects errors in the stored signal in a known manner. The error corrected signal is supplied to MPEG decoder 6 which includes therein a demultiplexer 61, control circuits 62 and 63, and random access memories 64 and 65. The digital signal is supplied to demultiplexer 61 which demultiplexes the signal into its respective video and audio components. The video signal is stored via control circuit 62 in memory 64, and the audio signal is stored via control circuit 63 in memory 65. Control circuits 62 and 63 decode the respective stored video and audio signals in a known manner and the decoded video and audio signals are supplied as, for example, analog video and audio output signals (after digital to analog conversion).

In addition to decoding the stored video and audio signals, control circuits 62 and 63 supply to a system control circuit 7 respective control signals that identify the storage states of the respective memories 64, 65. Similarly, memory control circuit 4 supplies to system control circuit 7 a control signal that identifies the storage state of memory 5. These control signals are sometimes identified as memory occupation data and generally identify how much data is stored in the respective memories. System control circuit 7, in response to the supplied control signals, controls the reproduction of the digital video/audio data by the reproducing device 1 so as to, *inter alia*, prevent the underflow and/or overflow of the memories.

In accordance with the present embodiment, DVD reproducing apparatus 100 includes a bit rate detecting block 8 which detects the bit rate of the reproduced data (to be further discussed). DVD reproducing apparatus 100 further includes a control circuit 301 which transmits the error corrected digital signal output by circuit 4 on bus 300 in accordance with the IEEE-1394 standard. In addition to supplying the error corrected digital video/audio signal to MPEG decoder 6, error correction and memory control circuit 4 supplies the error corrected digital video/audio signal to bit rate detecting block 8. Bit rate detecting block 8 detects the bit rate of the output signal in accordance with, for example, the flow chart shown in Fig. 6. Referring to Fig. 6, bit rate detecting block 8 detects the occurrence of a packet header at inquiry 1, and if a packet header is detected, the number of packets that have been previously detected (N) is incremented by 1 (i.e., $N = N + 1$) at instruction 2. If, however, a packet header is not detected at inquiry 1, then bit rate detecting block 8 performs no function, that is, waits until a packet header is detected. After incrementing the number of detected packets at instruction 2, it is determined, at inquiry 3, whether a countdown timer has reached a null (or 0) value (to be discussed) and instructions 4 through 7 are performed only if the countdown timer has reached its null value. The countdown timer initially is set for a period of 1 second and, thus, the number of detected packets that are received by bit rate detecting block 8 corresponds to the number of packets

of data that are received during a period of one second. Accordingly, the bit rate is determined at instruction 4 by multiplying the number of bits in each packet of data (e. g., 2048 bytes per packet x 8 bits per byte) by the number of detected packet headers (N). After the bit rate is detected, the countdown timer is reset to 1 second at instruction 5 and the detected number of packets N is reset to 0 at instruction 6. Finally, the calculated bit rate of the data (transmitted during a period of 1 second) is transmitted to control circuit 301 at instruction 7. Thus, bit rate detecting block 8 transmits the bit rate of the variable rate data every second. Of course, the bit rate can be detected and transmitted for a period other than every 1 second. Control circuit 301 calculates from the transmitted bit rate the number of units (previously discussed) that are required in accordance with the IEEE-1394 standard, and then the transmission band necessary to transmit the video/audio signal is "secured" also in accordance with the IEEE-1394 standard.

Referring to Fig. 9, during each 125 μsec transmission cycle of the IEEE-1394 bus 300, a secured transmission band, represented by the hatched portions, is requested by control circuit 301 and such transmission band corresponds to the required number of units of data for the particular detected bit rate of that data. The hatched portion of each cycle shown in Fig. 9 therefore is "secured" for the data that is to be transmitted by DVD reproducing apparatus 100 of the present invention. The unsecured transmission band (i.e., the non-hatched portions) of each cycle is therefore usable by other devices, for example, digital VCR 903 shown in Fig. 1.

Control circuit 301 secures the necessary transmission band for each cycle and subsequently transmits the digital signal supplied from error correction and memory control circuit 4 on the secured transmission band of bus 300. The digital signal is transmitted to a control circuit 302 which operates to control the bus communication in accordance with the IEEE-1394 standard, which control circuit 302 being included in, for example, a digital television receiver 200 that includes an MPEG decoder 9. Therefore, and in accordance with the present invention, variable bit rate data reproduced by DVD reproducing apparatus 100 is transmitted on a digital serial bus in accordance with the IEEE-1394 standard.

The transmitted video/audio data is supplied from control circuit 302 to MPEG decoder 9 which has a structure similar to that of MPEG decoder 6, but control circuits 92, 93 do not produce control signals that identify the storage state of memories 94, 95. The digital video/audio signal is supplied to a demultiplexer 91 which demultiplexes the signal into its respective video and audio components which are then stored via control circuits 92 and 93 in random access memories 94 and 95, respectively. The respective digital and audio signals are decoded by control circuits 92 and 93 and the decoded video and audio signals are supplied as, for example, respective digital video and audio signals.

As previously mentioned, control circuits 92 and 93 do not generate control signals that identify the storage states of memories 94 and 95. DVD reproducing apparatus 100 operates to MPEG decode the reproduced signal in MPEG decoder 6 and simultaneously transmit the reproduced signal on bus 300. Since MPEG decoder 9 is equivalent to MPEG decoder 6, and since control circuits 62 and 63 generate respective control signals representing the storage states of memories 64 and 65, which in turn controls the reproduction of the data from the digital video disk, it is unnecessary for control circuits 92 and 93 to generate controls signals that identify the respective storage states of memories 94 and 95. In other words, the storage states of memories 64 and 65 should be substantially equivalent to the storage states of memories 94 and 95, respectively and, thus, proper control of the reproduction of the digital video/audio data from the digital video disk is provided solely by MPEG decoder 6.

As previously mentioned, MPEG decoder 6 may supply as outputs respective analog video and audio signals and such signals may be supplied on an analog signal line 400 to an analog television receiver 500, such as shown in Fig. 4.

In accordance with the present embodiment, as discussed above, the storage states of memories 64 and 65 are detected and the reproduction operation of DVD reproducing apparatus 100 is controlled in accordance with such storage states thus preventing underflow and overflow of memories 64 and 65. By the use of MPEG decoder 6, a separate MPEG decoder 9, that is coupled to DVD reproducing apparatus 100 of the present invention via digital serial bus 300, does not need to determine whether an underflow or overflow condition of memories 94 and 95 exists. Furthermore, by detecting the bit rate of the supplied digital video/audio signal periodically in bit rate detecting block 8, variable rate data may be transmitted on a digital serial bus in accordance with the IEEE-1394 standard, even when such standard requires that the transmitted bit rate be known.

Referring next to Fig. 3 of the drawings, a block diagram of apparatus for transmitting digital video and audio data in accordance with another embodiment of the present invention is shown. Fig. 5 also illustrates the present embodiment, wherein DVD reproducing apparatus 100 is coupled to a digital television 200 including therein a display unit and MPEG decoder 9. Referring back to Fig. 3, DVD reproducing apparatus 100 includes a DVD reproducing device 1, an amplifier 2, a demodulator 3, an error correction and memory control circuit 4, a random access memory 5, a bit rate detecting block 8, a system control circuit 7 and a control circuit 301 and thus is similar to DVD reproducing apparatus 100 shown in Fig. 2, except the DVD reproducing device of the present embodiment does not include an internal MPEG decoder 6. In the present embodiment, circuits 1-5 operate in a manner identical to that of circuits 1-5 shown in Fig. 2, wherein digital video/audio data is reproduced from a digital video disk, demodulated, stored in mem-

ory 5, error corrected in circuit 4 and supplied as an error corrected digital video/audio signal to control circuit 301 via bit rate detecting block 8. Bit rate detecting block 8 operates in the same manner as that described above with respect to the embodiment shown in Fig. 2 (in accordance with the flow chart shown in Fig. 6) and, therefore, further description thereof is omitted herein. Also, like the embodiment shown in Fig. 2, control circuit 301 shown in Fig. 3 secures the necessary bandwidth in accordance with the bit rate detected by bit rate detecting block 8 and transmits on bus 300 the error corrected digital video/audio signal in accordance with the IEEE-1394 standard, all as previously discussed.

The transmitted digital video/audio signal is supplied to a control circuit 302 included in digital television receiver 200 which supplies the received signal to an MPEG decoder 9 which includes therein a demultiplexer 91, control circuits 92 and 93, and memories 94 and 95. Demultiplexer 91 demultiplexes the transmitted signal into its respective video and audio components, and stores the video data via control circuit 92 in memory 94 and stores the audio data via control circuit 93 in memory 95. Control circuits 92 and 93 MPEG decode the respective video and audio data to produce respective digital video and audio signals.

In accordance with the present embodiment, control circuits 92 and 93 detect the storage states (conditions) of memories 94 and 95, respectively (like control circuits 62 and 63 in Fig. 2) and generate therefrom respective control signals that are supplied to control circuit 302. Also in accordance with the present invention, the control signals supplied from control circuits 92 and 93 to control circuit 302 are transmitted from control circuit 302 on digital serial bus 300 to control circuit 301 in DVD reproducing apparatus 100.

In accordance with the IEEE-1394 standard, control circuits 301 and 302 each have a block structure as shown in Fig. 7, wherein each control circuit includes an Iso packet transmitting and receiving block 310, a bus control block 311, an information signal processing block 312 and a plug control register 313 located within bus control block 311. Iso packet transmitting and receiving block 310 performs isochronous communication for transmitting the video signal data and audio signal data, and bus control block 311 performs asynchronous communication for transmitting control signals. Data is transmitted between the Iso packet transmitting and receiving block 310 and information signal processing block 312 within each control circuit 301 and 302. In accordance with the IEEE-1394 standard, the Iso packet that is transmitted between control circuit 301 and 302 has the data structure as shown in Fig. 8.

Referring to Fig. 8, each Iso packet is formed from "quadlets" of data, each quadlet consisting of four bytes of information. The Iso packet includes a header, which includes therein the data length that is provided in the so-called first quadlet. The Iso packet header further includes in the second quadlet cyclic redundancy check

(CRC) codes for the information of the first quadlet. As shown, the packet header is comprised of the first and second quadlets, such packet header being transmitted at the beginning of packet transmission. A data field follows the packet header, and the cyclic redundancy check codes for the data field follows that data field.

Bus control block 311 of each control circuit 301 and 302 receives from the respective information processing block 312 the control signals that identify the storage states of memories 94 and 95. Such information is transmitted from one control circuit to another control circuit utilizing asynchronous communication. Typically, control circuit 302 transmits such control signals asynchronously to control circuit 301 which subsequently supplies the transmitted control signals to system control circuit 7. As previously mentioned, bus control block 311 of each control circuit 301, 302 includes a respective plug control register 313. Plug control register 313 sets values stored therein in accordance with the transmitted information, for example, the transmitted signals, and the various information generated by the particular equipment utilized, and Iso packet transmitting and receiving block 310 of the respective control circuit 301, 302 is controlled in accordance with the values stored in plug control register 313.

Finally, the control signals transmitted to system control circuit 7 from control 301 operate to control the reproducing operation of DVD reproducing circuit 1 in order to prevent underflow and overflow of memories 94 and 95.

Like the first embodiment previously discussed with reference to Fig. 2, the embodiment of Fig. 3 is operable to transmit variable rate data across a transmission line, for example, IEEE-1394 bus 300, which has a predetermined rate of transmission. Referring again to Fig. 9, the secured transmission band changes every cycle (or perhaps every other or every third cycle, etc.), such secured band being determined from the detected bit rate of the digital signal.

While the present invention has been particularly shown and described in conjunction with preferred embodiments thereof, it will be readily appreciated by those of ordinary skill in the art that various changes may be made without departing from the

scope of the invention. For example, the present invention, although described with reference to the IEEE-1394 standard and the use of MPEG decoders, is not limited to this standard and/or the use of MPEG decoders, but may be applied to other standards and/or other types of coders/decoders that produce/decode variable-rate data.

Therefore, it is intended that the appended claims be interpreted as including the embodiments described herein, the alternatives mentioned above, and all equivalents thereto.

Claims

1. Apparatus for transmitting variable rate data on a transmission line requiring a predetermined rate, comprising:

    detection means for detecting a data rate of variable rate data at predetermined intervals of time;
    means for establishing a transmission rate of said variable rate data in accordance with the detected data rate; and
    means for transmitting said variable rate data on said transmission line in accordance with the established transmission rate.

2. The apparatus of claim 1, wherein said means for establishing includes means for securing a bandwidth of said transmission line required to transmit said variable rate data having said detected data rate.

3. The apparatus of claim 2, wherein said transmission line has a plurality of cycles, and said detection means is operable to detect the data rate of said variable rate data to be transmitted during each of said cycles.

4. The apparatus of claim 3, wherein said means for securing a bandwidth is operable to secure a new bandwidth for each cycle of said transmission line in accordance with the detected data rate of said variable rate data to be transmitted during the respective cycle.

5. Apparatus for transmitting variable rate data on a transmission line having a predetermined rate, comprising:

    means for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
    processing means for processing the produced variable rate signal, said processing means including means for generating said control signal in accordance with a condition of processing of the produced variable rate signal by said processing means; and
    transmitting means for transmitting the variable rate signal on said transmission line.

6. The apparatus of claim 5, wherein said processing means is operable to MPEG decode the produced variable rate signal.

7. The apparatus of claim 5, wherein said processing means includes buffering means for buffering the produced variable rate signal, and said means for

generating said control signal generates said control signal representing a state of said buffering means.

8. The apparatus of claim 5, further comprising reception means for receiving the variable rate signal transmitted on said transmission line, said reception means including reception processing means for processing the received transmitted variable rate signal in a similar manner as said processing means processes the produced variable rate signal, said reception processing means not generating a control signal that controls the reproduction of the signal from the record medium.

9. The apparatus of claim 8, wherein said processing means and said reception processing means are both MPEG decoders.

10. Apparatus for transmitting variable rate data on a transmission line having a predetermined rate, comprising:

    means for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
    transmitting means for transmitting the variable rate signal on said transmission line; and
    reception means for receiving the variable rate signal transmitted on said transmission line, said reception means including reception processing means for processing the received transmitted variable rate signal, said reception processing means including means for generating said control signal in accordance with a condition of processing of the received transmitted variable rate signal by said reception processing means, said reception means further including reception transmitting means for transmitting the generated control signal to said transmitting means;
    wherein said transmitting means is operable to receive the transmitted control signal and to supply the received transmitted control signal to said means for controlling.

11. The apparatus of claim 10, wherein said reception processing means includes buffering means for buffering the received transmitted variable rate signal, and said means for generating said control signal generates said control signal representing a state of said buffering means.

12. The apparatus of claim 11, wherein said reception processing means is an MPEG decoder.

13. Apparatus for transmitting variable rate data on a transmission line requiring a predetermined rate,

comprising:

a bit rate detector for detecting a data rate of variable rate data at predetermined intervals of time; and
a bus controller for establishing a transmission rate of said variable rate data in accordance with the detected data rate, and for transmitting said variable rate data on said transmission line in accordance with the established transmission rate.

14. The apparatus of claim 13, wherein said bus controller is operable to secure a bandwidth of said transmission line required to transmit said variable rate data having said detected data rate.

15. The apparatus of claim 14, wherein said transmission line has a plurality of cycles, and said bit rate detector is operable to detect the data rate of said variable rate data to be transmitted during each of said cycles.

16. The apparatus of claim 15, wherein said bus controller is further operable to secure a new bandwidth for each cycle of said transmission line in accordance with the detected data rate of said variable rate data to be transmitted during the respective cycle.

17. Apparatus for transmitting variable rate data on a transmission line having a predetermined rate, comprising:

a reproducing device controller for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
a processor for processing the produced variable rate signal, said processor being operable to generate said control signal in accordance with a condition of processing of the produced variable rate signal by said processor; and
a transmission line controller for transmitting the variable rate signal on said transmission line.

18. The apparatus of claim 17, wherein said processor is an MPEG decoder.

19. The apparatus of claim 17, wherein said processor includes a data buffer for buffering the produced variable rate signal, and said control signal generated by said processor represents a state of said data buffer.

20. The apparatus of claim 17, further comprising a receiver for receiving the variable rate signal transmitted on said transmission line, said receiver including a reception processor for processing the received transmitted variable rate signal in a similar manner as said processor processes the produced variable rate signal, said reception processor not generating a control signal that controls the reproduction of the signal from the record medium.

21. The apparatus of claim 20, wherein said processor and said reception processor are both MPEG decoders.

22. Apparatus for transmitting variable rate data on a transmission line having a predetermined rate, comprising:

a reproducing device controller for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
a transmitter for transmitting the variable rate signal on said transmission line; and
a receiver for receiving the variable rate signal transmitted on said transmission line, said receiver including a reception processor for processing the received transmitted variable rate signal, said reception processor generating said control signal in accordance with a condition of processing of the received transmitted variable rate signal by said reception processor, said receiver further being operable to transmit the generated control signal to said transmitter;
wherein said transmitter is operable to receive the transmitted control signal and to supply the received transmitted control signal to said reproducing device controller.

23. The apparatus of claim 22, wherein said reception processor includes a data buffer for buffering the received transmitted variable rate signal, and said control signal generated by said reception processor represents a state of said data buffer.

24. The apparatus of claim 23, wherein said reception processor is an MPEG decoder.

25. Method of transmitting variable rate data on a transmission line requiring a predetermined rate, comprising the steps of:

detecting a data rate of variable rate data at predetermined intervals of time;
establishing a transmission rate of said variable rate data in accordance with the detected data rate; and
transmitting said variable rate data on said transmission line in accordance with the established transmission rate.

26. The method of claim 25, wherein said step of establishing is carried out by securing a bandwidth of said transmission line required to transmit said variable rate data having said detected data rate.

27. The method of claim 26, wherein said transmission line has a plurality of cycles, and said detecting step is carried out by detecting the data rate of said variable rate data to be transmitted during each of said cycles.

28. The method of claim 27, wherein said step of securing a bandwidth is carried out by securing a new bandwidth for each cycle of said transmission line in accordance with the detected data rate of said variable rate data to be transmitted during the respective cycle.

29. Method of transmitting variable rate data on a transmission line having a predetermined rate, comprising the steps of:

> controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
> processing the produced variable rate signal;
> generating said control signal in accordance with a condition of processing of the produced variable rate signal; and
> transmitting the variable rate signal on said transmission line.

30. The method of claim 29, wherein said processing step is carried out by MPEG decoding the produced variable rate signal.

31. The method of claim 29, wherein said processing step includes the step of buffering the produced variable rate signal in a buffer, and said generated control signal represents a state of said buffer.

32. The method of claim 29, further comprising the steps of receiving the variable rate signal transmitted on said transmission line, and processing the received transmitted variable rate signal in a similar manner as said variable rate signal is processed in said first processing step, wherein a control signal representing a condition of processing of the received transmitted variable rate signal similar to the previously generated control signal is not generated.

33. The method of claim 32, wherein said first and second processing steps are carried by respective MPEG decoders.

34. Method of transmitting variable rate data on a transmission line having a predetermined rate, comprising the steps of:
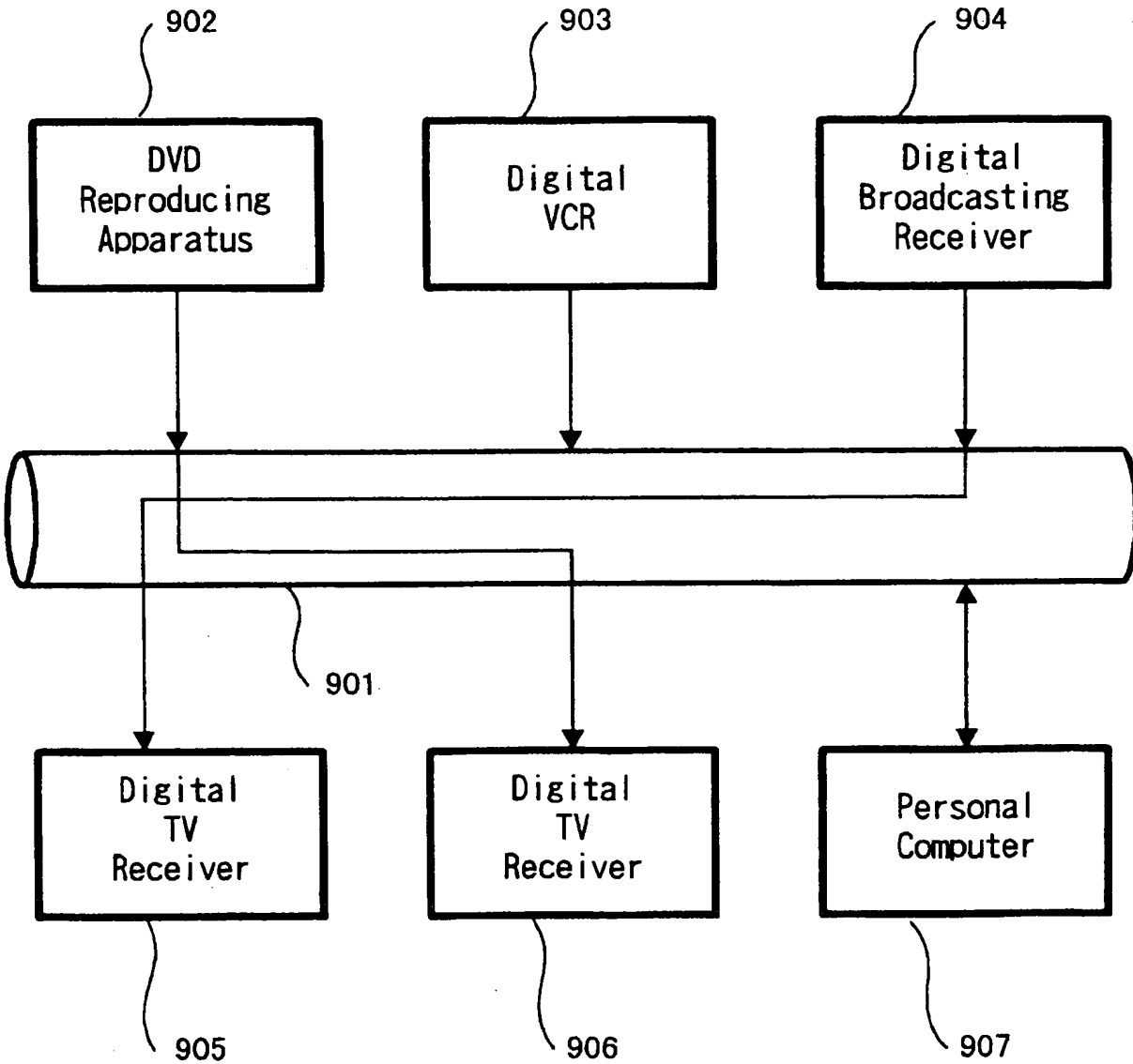
> controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal;
> transmitting from a transmission side the variable rate signal on said transmission line;
> receiving the variable rate signal transmitted on said transmission line;
> processing the received transmitted variable rate signal;
> generating said control signal in accordance with a condition of processing of the received transmitted variable rate signal;
> transmitting the generated control signal on said transmission line; and
> receiving at said transmission side the transmitted control signal;
> wherein the received transmitted control signal is utilized to control the reproducing by said controlling step.

35. The method of claim 34, wherein said processing step includes the step of buffering the received transmitted variable rate signal in a buffer, and the generated control signal represents a state of said buffer.

36. The method of claim 35, wherein said processing step is carried out by an MPEG decoder.
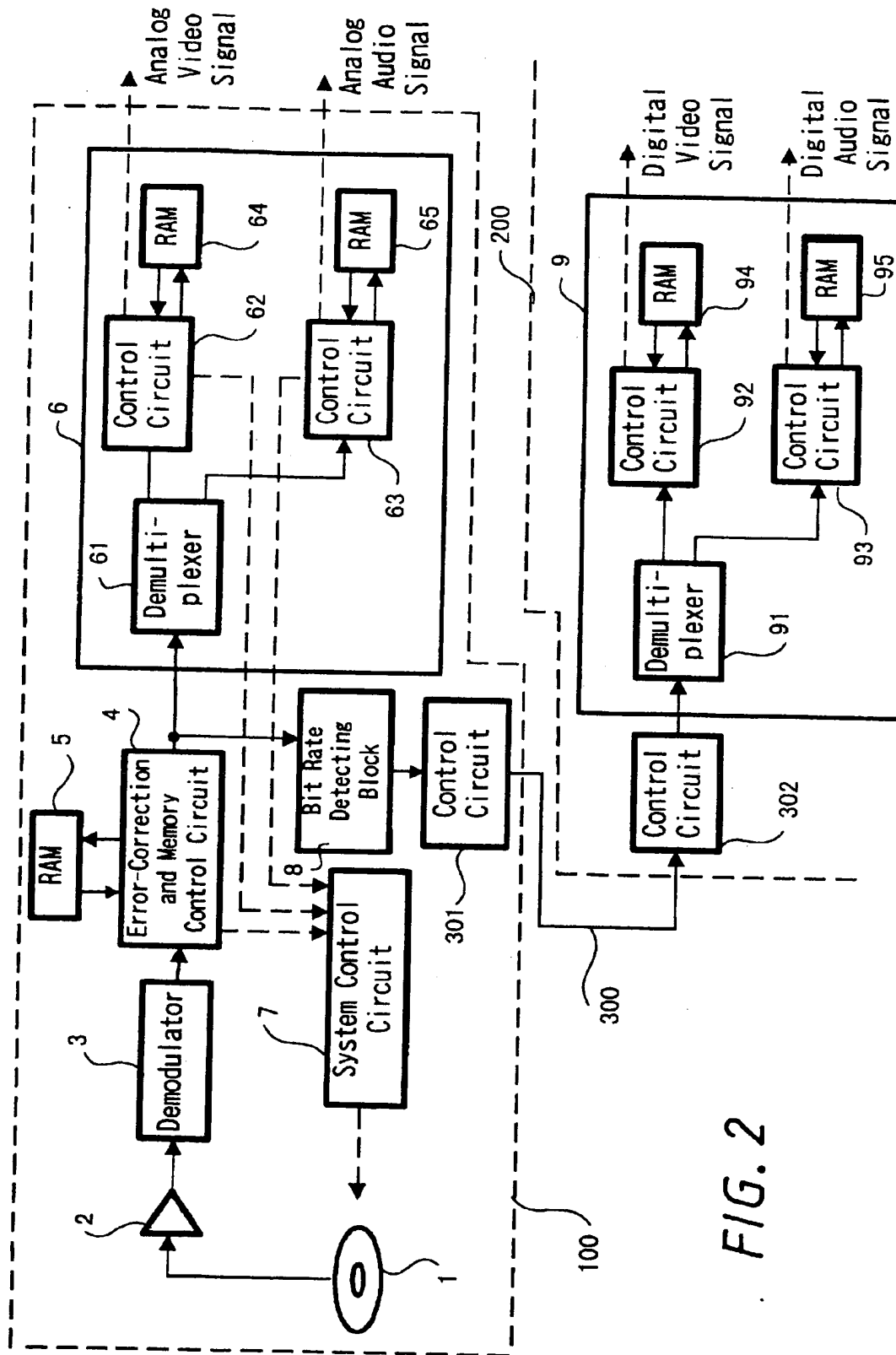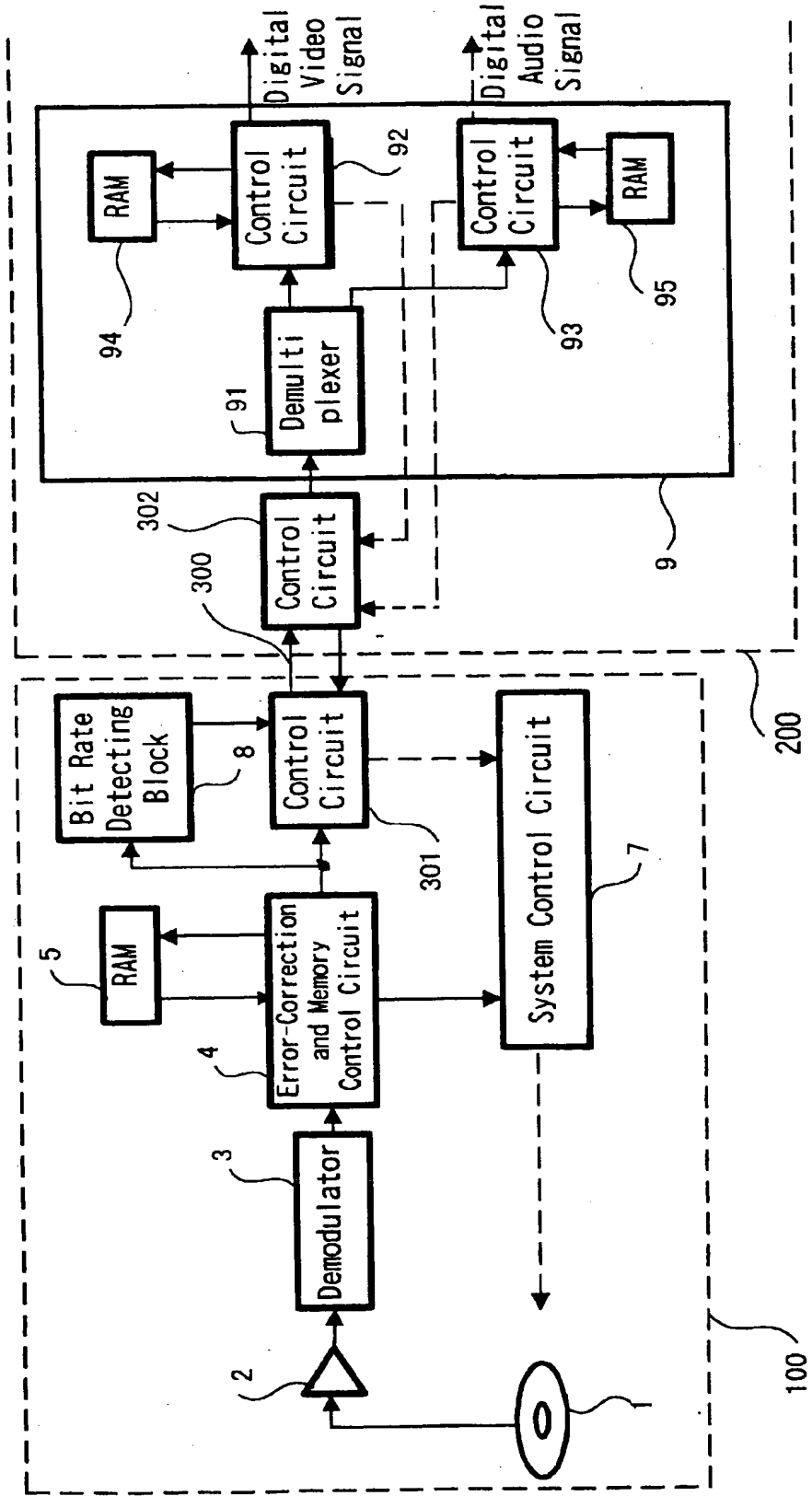
FIG. 1

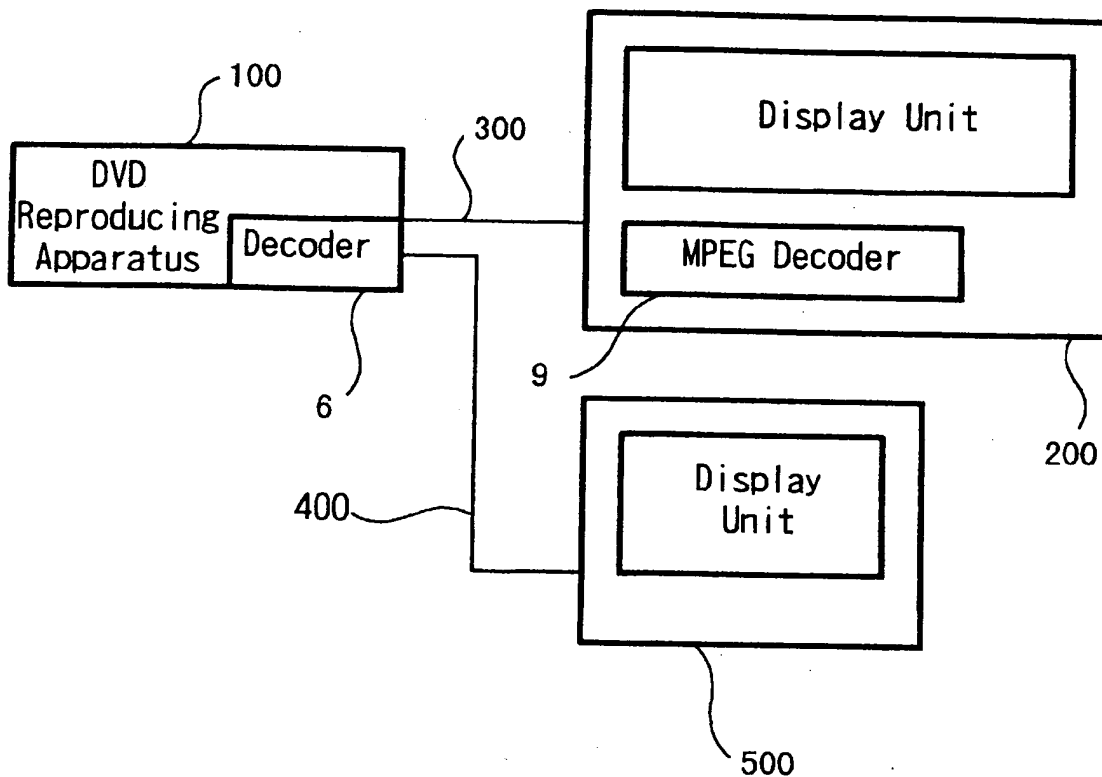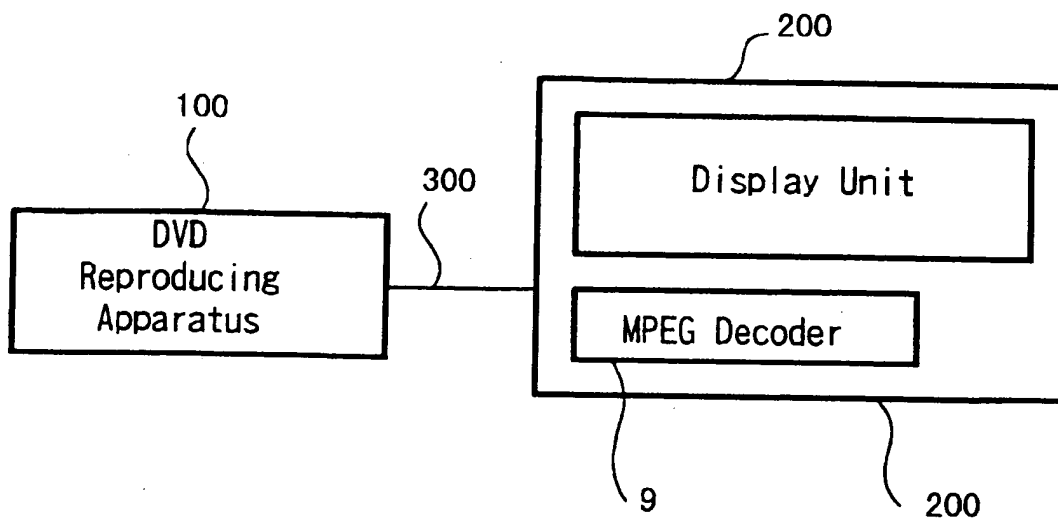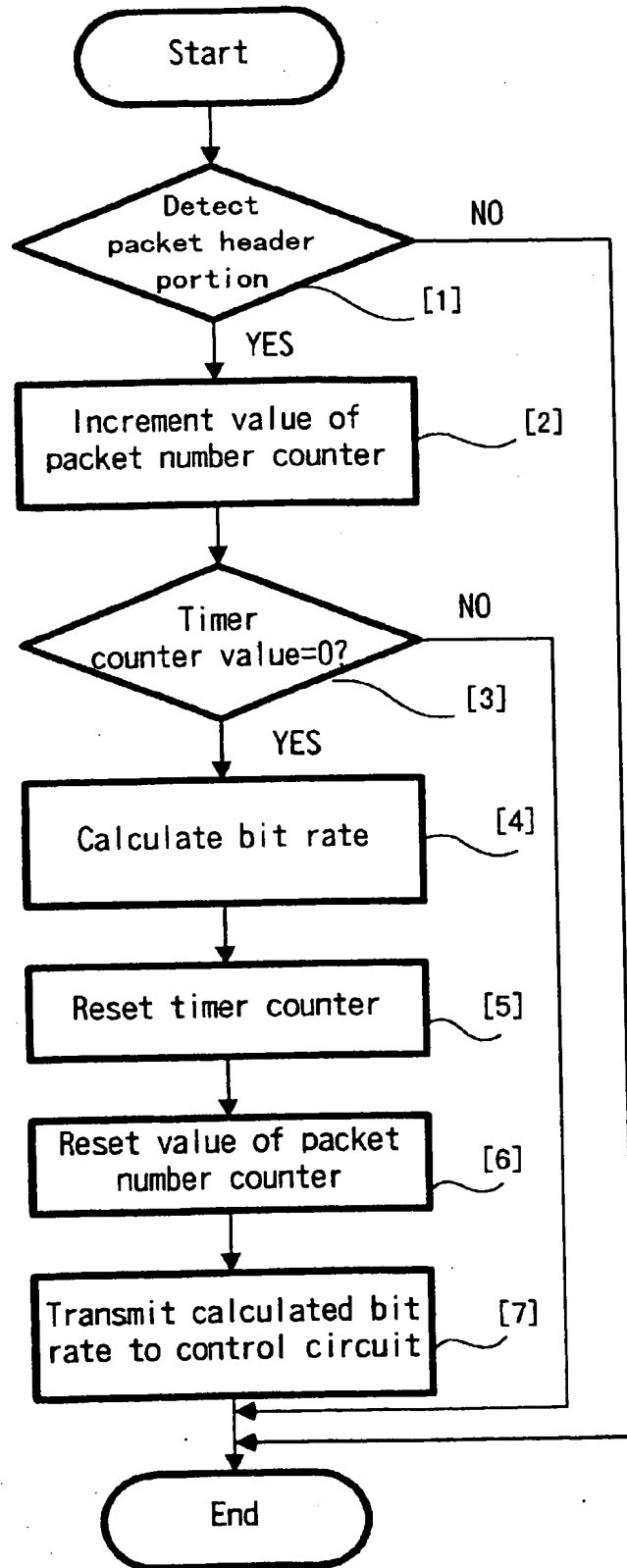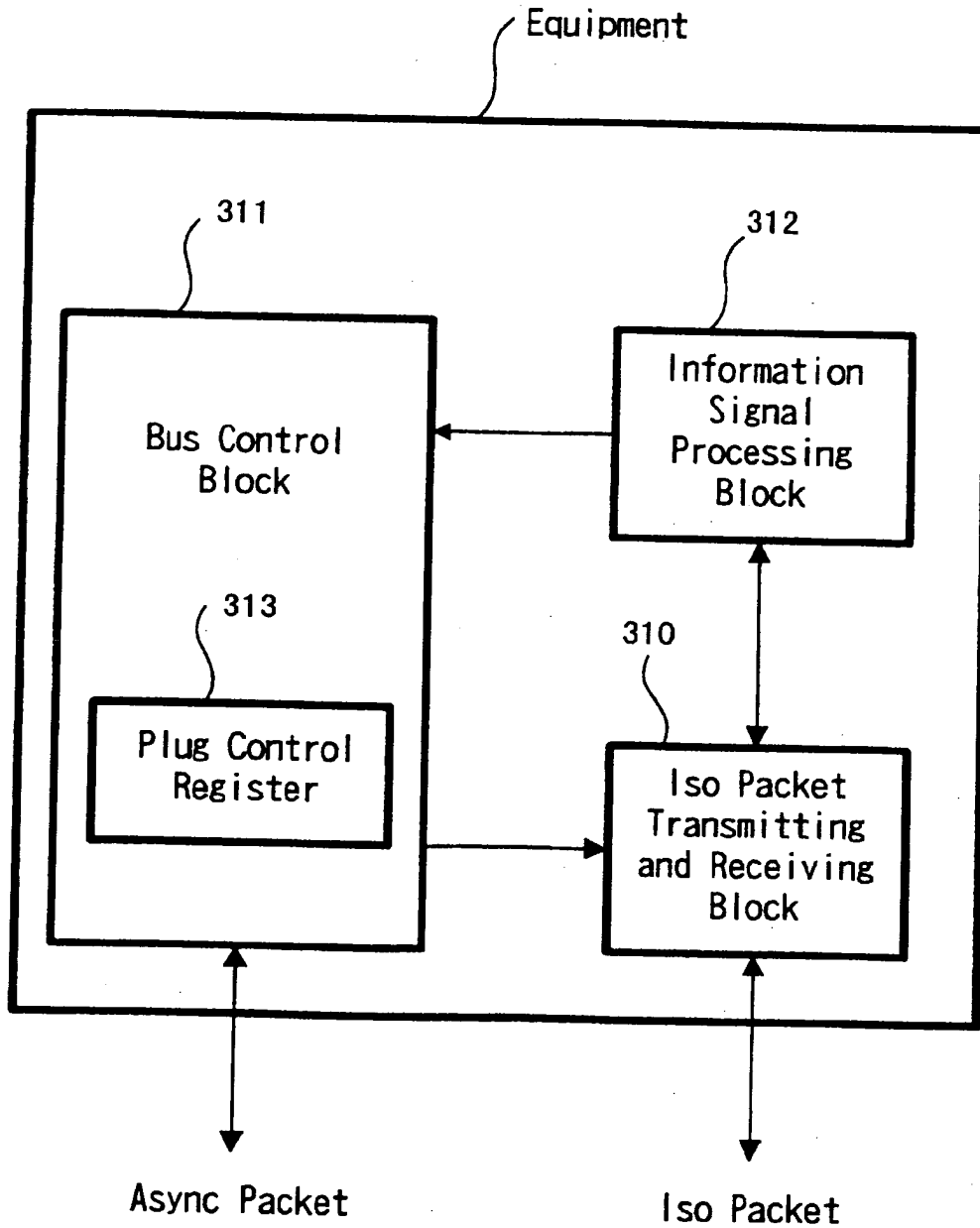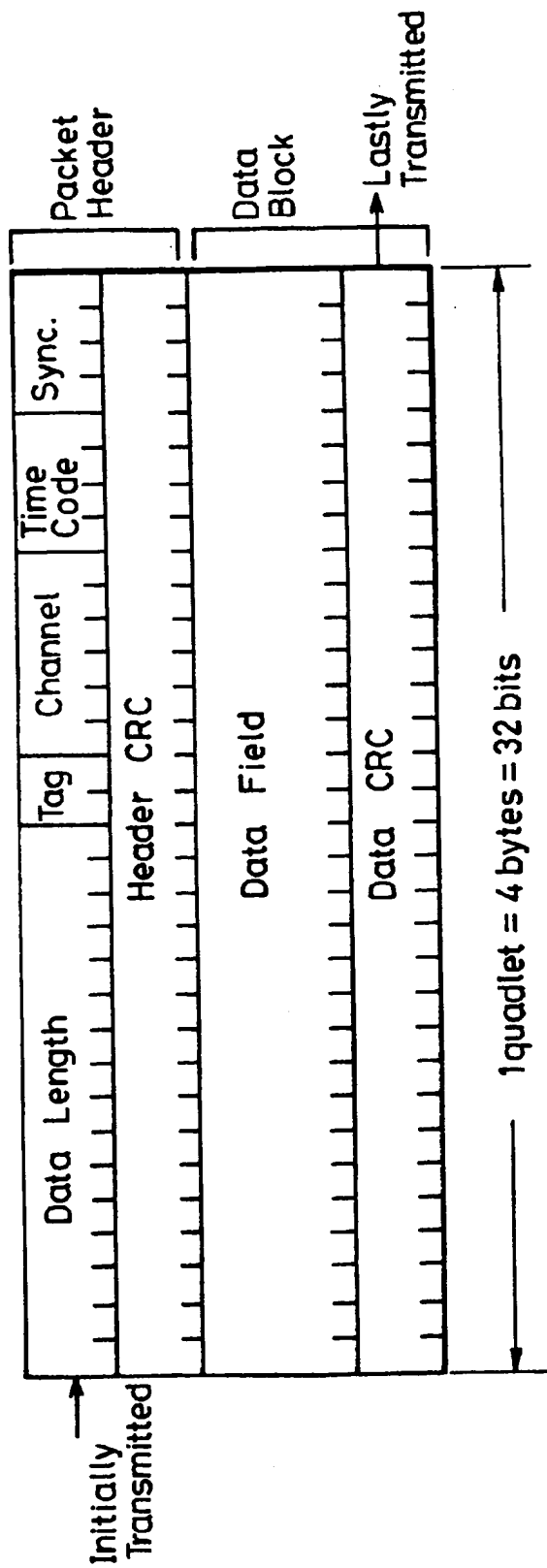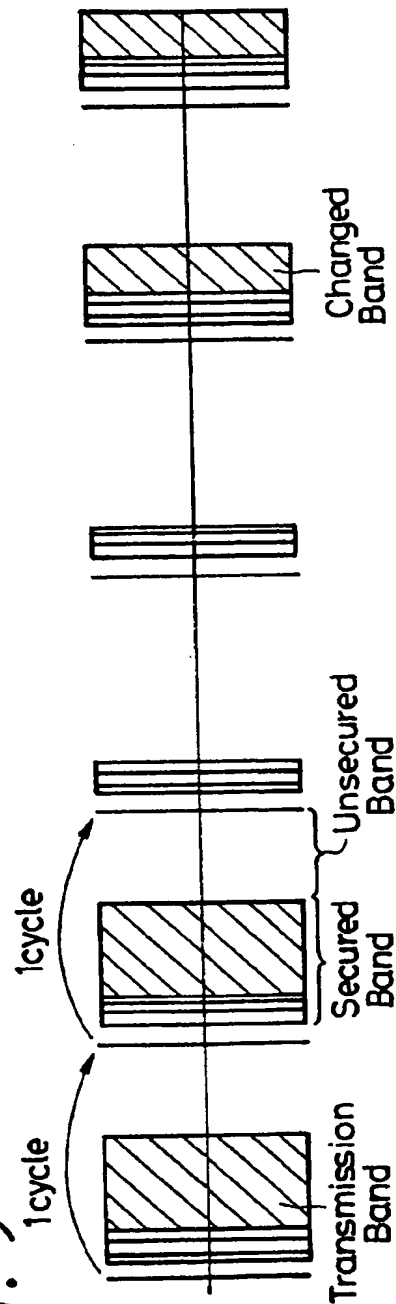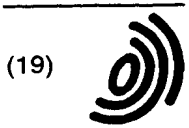902 DVD Reproducing Apparatus

903 Digital VCR

904 Digital Broadcasting Receiver

901

905 Digital TV Receiver

906 Digital TV Receiver

907 Personal Computer

FIG. 2

FIG. 3

FIG. 4

FIG. 5

FIG. 6

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                    ┌─────────────┐
                    │    Start    │
                    └──────┬──────┘
                           │
                           ▼
                    ╱──────────────╲            NO
                   ╱  Detect         ╲──────────────┐
                   ╲  packet header  ╱              │
                    ╲  portion      ╱   [1]         │
                     ╲─────┬───────╱                │
                           │ YES                    │
                           ▼                        │
                   ┌──────────────────┐             │
                   │ Increment value of│   [2]      │
                   │ packet number     │            │
                   │ counter           │            │
                   └────────┬──────────┘            │
                            │                       │
                            ▼                       │
                    ╱──────────────╲        NO      │
                   ╱   Timer         ╲──────────────┤
                   ╲  counter value=0?╱             │
                    ╲────────┬───────╱   [3]        │
                             │ YES                  │
                             ▼                      │
                   ┌──────────────────┐             │
                   │ Calculate bit rate│  [4]       │
                   └────────┬──────────┘            │
                            │                       │
                            ▼                       │
                   ┌──────────────────┐             │
                   │ Reset timer      │   [5]       │
                   │ counter          │            │
                   └────────┬──────────┘            │
                            │                       │
                            ▼                       │
                   ┌──────────────────┐             │
                   │ Reset value of   │   [6]       │
                   │ packet number    │            │
                   │ counter          │            │
                   └────────┬──────────┘            │
                            │                       │
                            ▼                       │
                   ┌──────────────────┐             │
                   │ Transmit calculated│  [7]      │
                   │ bit rate to        │           │
                   │ control circuit    │           │
                   └────────┬──────────┘            │
                            │◄─────────────────────┘
                            ▼
                    ┌─────────────┐
                    │    End      │
                    └─────────────┘
```

FIG. 7

Equipment

311

Bus Control
Block

313

Plug Control
Register

312

Information
Signal
Processing
Block

310

Iso Packet
Transmitting
and Receiving
Block

Async Packet

Iso Packet

FIG. 8

Packet Header: Tag | Channel | Time Code | Sync.

Data Length

Header CRC

Data Block:

Data Field

Data CRC

1 quadlet = 4 bytes = 32 bits

Initially Transmitted

Lastly Transmitted

FIG. 9

1 cycle | 1 cycle

Transmission Band

Secured Band

Unsecured Band

Changed Band

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EUROPEAN PATENT APPLICATION

(12)

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(54) **Apparatus and methods for transmitting data**

(57) DVD reproducing apparatus (100) transmits variable-bit rate data, on a digital serial bus (300) at a predetermined transmission rate, by reproducing data from a record medium (1) in accordance with a control signal to produce the variable rate data. The data rate of the variable rate data is detected (8) at predetermined intervals of time, the rate of transmission of the variable rate data is established in accordance with the detected data rate, and the variable rate data is transmitted in accordance with the established transmission rate. The DVD reproducing apparatus (100) may include an MPEG decoder (6) which MPEG decodes the reproduced data and which generates the control signal in accordance with amounts of data stored within various buffers, such control signal being utilized to control the reproduction of the data from the record medium (1). A receiver, e.g., a digital television (200), having an MPEG decoder (9) therein receives the transmitted data and MPEG decodes the data, but such MPEG decoder (9) does not generate a control signal similar to the previously generated control signal in order to prevent underflow/overflow of the memories therein. In another embodiment, the DVD reproducing apparatus (100) does not include an MPEG decoder, but the receiving device's MPEG decoder (9) generates a control signal that is transmitted back to the DVD reproducing apparatus (100) in order to prevent underflow/overflow of the memories within the receiving device's MPEG decoder.
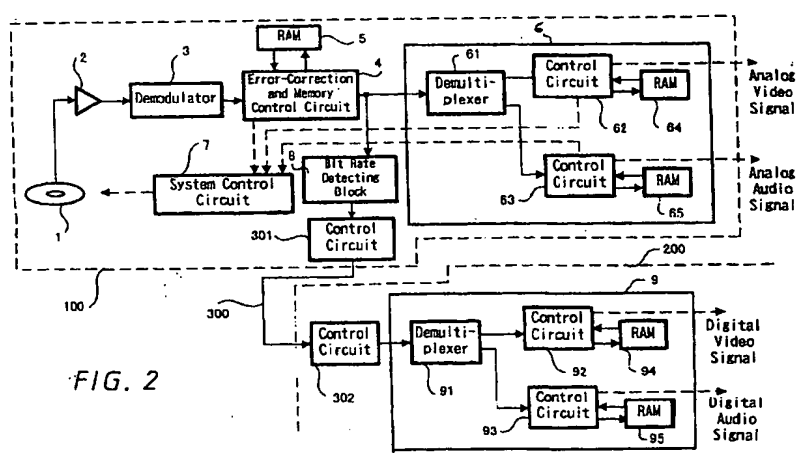
FIG. 2

	European Patent Office	**EUROPEAN SEARCH REPORT**	**Application Number** EP 97 30 6292

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	LAUDERDALE J ET AL: "USING THE MINIMUM RESERVATION RATE FOR TRANSMISSION OF PRE-ENCODED MPEG VBR VIDEO USING CBR SEVICE" IEICE TRANSACTIONS ON COMMUNICATIONS,JP,INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG. TOKYO, vol. E79-B, no. 8, 1 August 1996 (1996-08-01), pages 1023-1029, XP000628639 ISSN: 0916-8516 * section 1 "Introduction" * * section 2 "System model" * * Introduction of section 3 "The minimum reservation rate" * * abstract *	1-4, 13-16, 25-28	H04N7/52 H04N7/24 G11B20/10 H04L25/02 G11B20/00
X	LAUDERDALE J ET AL: "A NEW TECHNIQUE FOR TRANSMISSION OF PRE-ENCODED MPEG VBR VIDEO USING CBR SERVICE" IEEE INTERNATIONAL CONFERENCE ON COMMUNICATIONS (ICC),US,NEW YORK, IEEE, 23 June 1996 (1996-06-23), pages 1416-1420, XP000625043 ISBN: 0-7803-3251-2 * section 1 "Introduction" * * section 2 "System model" *	1-4, 13-16, 25-28	**TECHNICAL FIELDS SEARCHED (Int.Cl.6)** H04N G11B H04L G06F H04J
P,X	WO 96 34477 A (YAMADA MASAZUMI ;IITSUKA HIROYUKI (JP); MATSUSHITA ELECTRIC IND CO) 31 October 1996 (1996-10-31)	1-4, 13-16, 25-28	
E	-& EP 0 862 295 A (MATSUSHITA ELECTRIC IND CO) 2 September 1998 (1998-09-02) * the whole document *	1-4, 13-16, 25-28	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 September 2000	La, V

EPO FORM 1503 03.82 (P04C01)

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European Patent
Office

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 97 30 6292

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	WO 95 12274 A (TIME WARNER ENTERTAINM CO LP) 4 May 1995 (1995-05-04)	5-7, 10-12, 17-19, 22-24, 29-31, 34-36	
Y	* page 10, line 1 - page 16, line 26 * * figure 2 *	8,9,20, 21,32,33	
Y A	EP 0 658 010 A (SONY CORP) 14 June 1995 (1995-06-14) * the whole document *	8,9,20, 21,32,33 1-5, 13-17, 25-29	
A	EP 0 632 671 A (IBM) 4 January 1995 (1995-01-04) * column 8, line 39 - column 14, line 36 * * abstract *	1-4, 13-16, 25-28	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 474 (E-692), 12 December 1988 (1988-12-12) & JP 63 191436 A (FUJITSU LTD), 8 August 1988 (1988-08-08) * abstract *	1-4, 13-16, 25-28	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 September 2000	La, V

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-4,13-16,25-28

   Apparatus for transmitting variable rate data on a transmission line requiring a predetermined rate, comprising a detection means for detecting a data rate of variable rate data at predetermined intervals of time, a means for establishing a transmission rate of said variable rate data in accordance with the detected data rate, and a means for transmitting said variable rate data on said transmission line in accordance with the established transmission rate.

2. Claims: 5-9,17-21,29-33

   Apparatus for transmitting variable rate data on a transmission line having a predetermined rate, comprising a means for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal, a processing means for processing the produced variable rate signal and including a means for generating said control signal, and a transmitting means for transmitting the variable rate signal on said transmission line.

3. Claims: 10-12,22-24,34-36

   Apparatus for transmitting variable rate data on a transmission line having a predetermined rate, comprising a means for controlling the reproducing of a signal from a record medium in accordance with a control signal to produce a variable rate signal, a transmitting means for transmitting the variable rate signal on said transmission line, and a reception means for receiving the variable rate signal transmitted on said transmission line and including a reception processing means for processing the received transmitted variable rate signal, said reception processing means including a means for generating said control signal and a means for transmitting the generated control signal to said transmitting means which will supply the control signal to said means for controlling.

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 97 30 6292

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PANCHA P ET AL: "BANDWIDTH REQUIREMENTS OF VARIABLE BIT RATE MPEG SOURCES IN ATM NETWORKS" PROCEEDINGS OF THE ANNUAL JOINT CONFERENCE OF THE COMPUTER AND COMMUNICATIONS SOCIETIES (INFOCOM),US,LOS ALAMITOS, IEEE COMP. SOC. PRESS, vol. CONF. 12, 28 March 1993 (1993-03-28), pages 902-909, XP000419649 ISBN: 0-8186-3580-0 * section 1.0 "Introduction" * * section 2.0 "MPEG source characteristics" * * section 3.0 "Predicting source traffic"*	1-4, 13-16, 25-28	
A	EP 0 633 570 A (SONY CORP) 11 January 1995 (1995-01-11) * section "Summary of the invention" * * abstract *	5-12, 17-24, 29-36	
A	EP 0 703 713 A (SONY CORP) 27 March 1996 (1996-03-27) * figures 1,2,6 *	1-36	TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 September 2000	La, V

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 97 30 6292

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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26-09-2000

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 9634477	A	31-10-1996	JP	8307453 A	22-11-1996
			JP	8340338 A	24-12-1996
			JP	9046390 A	14-02-1997
			AU	5513896 A	18-11-1996
			BR	9608322 A	23-02-1999
			CN	1183187 A	27-05-1998
			EP	1009186 A	14-06-2000
			EP	1009187 A	14-06-2000
			EP	1009188 A	14-06-2000
			EP	0862295 A	02-09-1998
WO 9512274	A	04-05-1995	US	5576843 A	19-11-1996
			AU	703544 B	25-03-1999
			AU	3837797 A	08-01-1998
			AU	687456 B	26-02-1998
			AU	7982494 A	22-05-1995
			CA	2174320 A	04-05-1995
			CA	2237075 A	04-05-1995
			DE	726012 T	02-01-1998
			EP	0726012 A	14-08-1996
			EP	0971354 A	12-01-2000
			EP	0971357 A	12-01-2000
			JP	11205749 A	30-07-1999
			JP	2892159 B	17-05-1999
			JP	9500508 T	14-01-1997
			US	5671320 A	23-09-1997
			US	5712950 A	27-01-1998
			US	6115534 A	05-09-2000
EP 0658010	A	14-06-1995	JP	7222263 A	18-08-1995
			CN	1115928 A	31-01-1996
EP 0632671	A	04-01-1995	US	5581703 A	03-12-1996
			JP	2601993 B	23-04-1997
			JP	7073121 A	17-03-1995
			US	5701465 A	23-12-1997
JP 63191436	A	08-08-1988	NONE		
EP 0633570	A	11-01-1995	JP	7029308 A	31-01-1995
			DE	69420634 D	21-10-1999
			DE	69420634 T	30-12-1999
			US	5519681 A	21-05-1996
EP 0703713	A	27-03-1996	JP	8097837 A	12-04-1996
			US	5781599 A	14-07-1998

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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